Confinuous etching method and apparatus therefor.

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Patent Number:	EP0429270
Publication date:	1991-05-29
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Requested Patent:	□ <u>EP0429270</u> , <u>B1</u>
Application Number:	EP19900312550 19901119
Priority Number(s):	JP19890301618 19891120
IPC Classification:	G03F7/36
EC Classification:	G03F7/36
EC Classification:	G03F7/36
Equivalents:	DE69028180D, DE69028180T, JP2926798B2,
	KR9311905, US5127987
Abstract	

A plurality of resist membranes are formed on a semiconductor wafer to be etched. The top resist is patterned by light beam, laser beam, X-rays, or electron beams to form a mask. The wafer is transferred to a first unit (2) into which discharging gas is introduced and plasma is generated in order to dry-etch the multilayer resists. The multilayer is transferred to a second unit (3) in a vacuum. In the second unit, the membrane of the wafer is dry-etched to a predetermined depth. The wafer then is transferred to a third unit (4) in a vacuum where part of the resist is removed according to the mask pattern and treatment of the resist by the plasma.